What is claimed is:

1. A circuit for converting an analog capacitive transducer signal to a digital signal comprising:

a first circuit for generating a digital signal that can vary in frequency, the capacitive transducer being connected to the digital signal generator, whereby a change of capacitance in the transducer causes the frequency of the digital signal generator to vary;

a second circuit for generating a delta-sigma bit stream that can vary in density, whereby changes in the frequency of the digital signal generator causes the density of the delta-sigma bit stream to vary proportionally.

2. The circuit according to claim 1, wherein the capacitive transducer is a continuously variable capacitor.

3. The circuit according to claim 1, wherein the first circuit is an oscillator wherein the capacitance of the capacitive transducer controls the oscillator's oscillation frequency.

4. The circuit according to claim 3, wherein the oscillator is a ring oscillator.

5. The circuit according to claim 3, wherein the oscillator is a relaxation oscillator.

6. The circuit according to claim 1, wherein the second circuit is a frequency delta-sigma modulator.

7. The electronic circuit according to claim 6, wherein the frequency delta-sigma modulator uses modulo-2 arithmetic.

8. The electronic circuit according to claim 6, wherein the frequency delta-sigma modulator is comprised of an edge-counter using a high frequency clock signal and a modulo-2 exclusive OR differentiator.

9. The circuit according to claim 6, wherein the frequency delta-sigma modulator has an order of one or higher.

10. The circuit according to claim 1, wherein the second circuit includes an internal oscillator for sampling.

11. The circuit according to claim 1, wherein the second circuit uses an external signal for sampling.

12. The circuit according to claim 11, wherein the external signal for sampling is provided by an external digital signal processing unit.

13. The circuit according to claim 12, wherein the external digital signal processing unit includes facilities for decimation and filtering of the bit stream from the second circuit.

14. The circuit according to claim 1 further comprising bond pads for wiring the first circuit to the capacitive transducer.

15. The circuit according to claim 1, wherein the capacitive transducer is monolithically integrated with the conversion circuit.

16. The circuit according to claim 1 further comprising bond pads for wiring the external digital signal processing unit to the second circuit to the external digital signal processing unit.

17. The circuit according to claim 1, wherein the external digital signal processing unit is monolithically integrated with the conversion circuit.

18. The circuit according to claim 1, wherein the frequency modulation block and frequency to delta-sigma bit stream conversion block are realized using digital CMOS circuit components.

19. The circuit according to claim 18, wherein the digital CMOS circuit components are realized using the same fabrication process used to make the external digital signal processing unit.

20. The circuit according to claim 1 further comprising an external digital signal processing unit receiving the delta-sigma bit stream generated by the second circuit.

21. An electronic circuit for the detection and conversion of a capacitive transducer signal comprising:

a frequency modulation block;

a frequency to delta-sigma bit stream conversion block receiving the output of the frequency modulation block;

an external capacitor connected to the frequency modulation block; and

an external digital signal processing unit receiving the output of the frequency to delta-sigma bit stream conversion block;

whereby a change of capacitance in the external capacitor causes a change in oscillation frequency within the frequency modulation block, and

whereby the change in oscillation frequency causes a change in the output bit stream of the frequency to delta-sigma bit stream conversion block.

22. The electronic circuit according to claim 21, wherein the external capacitor is a continuously variable capacitor.

23. The electronic circuit according to claim 21, wherein the frequency modulation block is an oscillator, and wherein the external capacitor controls the oscillation frequency.

24. The electronic circuit according to claim 21, wherein the oscillator is a ring oscillator.

25. The electronic circuit according to claim 21, wherein the frequency to delta-sigma bit stream conversion block is a frequency delta-sigma modulator.

26. The electronic circuit according to claim 25, wherein the frequency delta-sigma modulator uses modulo-2 arithmetic.

27. The electronic circuit according to claim 25, wherein the frequency delta-sigma modulator has an order of one or higher.

28. The electronic circuit according to claim 21, wherein the frequency to delta-sigma bit stream conversion block includes an internal oscillator for sampling.

29. The electronic circuit according to claim 21, wherein the frequency to delta-sigma bit stream conversion block requires an external signal for sampling.

30. The electronic circuit according to claim 29, wherein the external signal for sampling is provided by the external digital signal processing unit.

31. The electronic circuit according to claim 21, wherein the external digital signal processing unit includes facilities for decimation and filtering of the bit stream from the frequency to delta-sigma bit stream conversion block.

32. The electronic circuit according to claim 21, wherein the external capacitor is connected to the frequency modulation block using bond pads for wiring to the external capacitor.

33. The electronic circuit according to claim 21, wherein the external capacitor is connected to the frequency modulation block using monolithic integration of the electronic circuit with the external capacitor.

34. The electronic circuit according to claim 21, wherein the external digital signal processing unit is connected to the frequency to delta-sigma bit stream conversion block by bond pads for wiring to the external digital signal processing unit.

35. The electronic circuit according to claim 21, wherein the external digital signal processing unit is connected to the frequency to delta-sigma bit stream conversion block using monolithic integration of the electronic circuit with the external digital signal processing unit.

36. The electronic circuit according to claim 21, wherein the frequency modulation block and frequency to delta-sigma bit stream conversion block are comprised of digital CMOS circuit components.

37. The electronic circuit according to claim 36, wherein the digital CMOS circuit components are formed using the same fabrication process used to make the external digital signal processing unit.

38. A circuit for converting an analog capacitive transducer signal to a digital signal comprising:

a first circuit for generating a digital signal that can vary in frequency, the capacitive transducer being connected to the digital signal generator, whereby a change of capacitance in the transducer causes the frequency of the digital signal generator to vary;

a second circuit for generating a delta-sigma bit stream that can vary in density, the second circuit receiving the frequency varying digital signal from the first circuit, whereby changes in the frequency of the digital signal generator causes the density of the delta-sigma bit stream to vary proportionally; and

an external digital signal processing unit receiving the delta-sigma bit stream from the second circuit for further processing.

39. A circuit for converting an analog transducer signal into a digital signal comprising:

a first circuit for generating a digital signal that can vary in frequency, the transducer being connected to the digital signal generator, whereby a change in the transducer's characteristics or output causes the frequency of the digital signal generator to vary; and

a second circuit for generating a delta-sigma bit stream that can vary in density, whereby changes in the frequency of the digital signal generator causes the density of the delta-sigma bit stream to vary proportionally.